REMARKS

This Amendment responds to the Office Action dated March 8, 2004 in which the Examiner required a new title, objected to claim 10 and rejected claims 1-26 under 35 U.S.C. §102(b).

As indicated above, a new title has been provided which clearly indicates the invention to which the claims are directed. Applicants respectfully request the Examiner approves the new title.

As indicated above, a copy of the claims has been provided. As indicated in the claims, the period at the end of claim 10 which was inadvertently omitted in the previous response, is now present as in the original claim. Therefore, Applicants respectfully request the Examiner withdraws the objection to claim 10.

Claim 1 and 11 claim a data processing system comprising a plurality of processors and a memory. The plurality of processors executes a series of different types of processing functions on data to be processed in a prescribed order. Each processor executes a processing function different from one another. The data to be processed is image data that consists of a plurality of pixel data. The memory stores the data to be processed in association with state information representing the processing to be performed next for each pixel data to be processed. Processing functions are asynchronously executed on the data to be processed by the plurality of processors. One processing is executed on each pixel data by one processor at a time. The plurality of processors shares the memory.

Through the structure of the claimed invention having a) a memory which stores state information representing processing to be performed next and b)

executing processing on each pixel data by one processor at a time, as claimed in claims 1 and 11, the claimed invention provides a data processing system capable of processing data at high speed while allowing memory capacity to be reduced. The prior art does not show, teach or suggest the invention as claimed in claims 1 and 11.

Claim 25 claims a data processing device and claim 26 claims an image processing device. The device is comprises first and second (image) processors and a memory. The first (image) processor executes first (image) processing on data. The second (image) processor executes second (image) processing on the data that is subjected to the first processing. The memory stores the (image) data in association with state information to represent the processing state of the (image) data. The first and second (image) processors are asynchronously executed on the (image) data by the first and second (image) processors. The first and second (image) processors share the memory.

Through the structure of the claimed invention having a second (image) processor which executes (image) processing on the (image) data subjected to the first (image) processing, and having a memory store state information representing the processing state of the (image) data, as claimed in claims 25 and 26, the claimed invention provides a data processing system an image processing device capable of processing data at a high speed while allowing the memory capacity to be reduced. The prior art does not show, teach or suggest the invention as claimed in claims 25 and 26.

Claim 1-26 were rejected under 35 U.S.C. §102(b) as being anticipated by *Kuo et al* (U.S. Patent No. 5,299,309).

Kuo et al. appears to disclose a graphics control system for a computer system which improves the processing efficiency of the computer, especially when the computer is displaying windows. (col. 1, lines 9-12) As shown in FIG. 1, this conventional graphics control system comprises a host computer 10, a graphics processor 20, a display memory 30, and a display device, such as CRT 32. The host computer 10 comprises a main memory 12 and a CPU 14. All commands relating to the windows display are generated by the host computer 10 which communicates with the graphics processor 20 via the bus 16. The graphics processor 20 is comprised of a processing unit 22, a graphics context 24, and a drawing unit 26. The processing unit 22 performs two functions: 1) it receives and executes the commands issued by the host computer 10; and 2) it converts certain graphics parameters stored in the graphics context 24 into display data. (col. 1, lines 20-33) The graphics context 24 is a buffer that stores a set of image parameters needed to carry out a current command. For example, to draw a line segment on the CRT 32, the graphics context 24 stores the initial and final addresses of the line segment on the CRT, information relating to foreground color and background color, information relating to the mix of the three primary colors red, green, and blue, and other similar parameters. When displaying windows, other parameters will also need to be stored, such as the manner in which overlapping images will be processed (i.e., whether by AND or NOR processing), the initial and final addresses of the windows on the CRT, etc. (col. 1, lines 40-52) The improved graphics control system comprises a shared memory which is directly accessible by both the host computer and by the graphics processor. Because the shared memory is directly accessible by the host computer and by the graphics processor, the host computer can write the graphics context

parameters of a next command into the shared memory while the graphics processor is executing a current command. When the graphics processor completes execution of the current command, it can receive the graphics context parameters of the next command to be executed directly from the shared memory. Because the host computer is able to store the next set of graphics context parameters in the shared memory while a current command is being executed, the host computer does not have to wait until completion of the current command before computing the graphics context parameters for the next command and entering them in the graphics processor. Thus, the host computer will not have to access the graphics processor so frequently when the graphics context needs to be changed. (col. 2, lines 46-68)

Thus, *Kuo et al.* merely discloses a CPU 14 which writes graphic contents parameters into a shared memory where the graphic context parameters include initial and final addresses of a line segment, information relating to foreground color and background color, information relating to the mix of the three primary colors, etc. (col. 1, lines 43-48) Thus, nothing in *Kuo et al.* shows, teaches or suggests a) each of a plurality of processors executes a processing function on pixel data as claimed in claims 1 and 11 or b) a second (image) processor executes second (image) processing on (image) data that is subjected to first (image) processing as claimed in claims 25 and 26. Rather, the CPU 14 of *Kuo et al.* writes the graphic context parameters into a shared memory (i.e., the graphic context parameters of *Kuo et al.*, which are output by CPU14 are not pixel data and are not processed on data subjected to first processing).

Additionally, *Kuo et al.* merely discloses a shared memory storing graphic context parameters such as initial and final addresses of a line segment, information

relating to foreground and background color, information relating to the mix of three primary colors, etc. Nothing in *Kuo et al.* shows, teaches or suggests a memory storing state information representing processing to be performed next as claimed in claims 1 and 11 or state information representing the processing state of the data as claimed in claims 25 and 26. Rather, *Kuo et al.* merely discloses a shared memory storing graphic context parameters representing the initial and final addresses of a line segment, information relating to foreground and background color, information relating to the mix of the three primary colors, etc.

Since nothing in *Kuo et al.* shows, teaches or suggests a) each processor executes a processing function on pixel data and a memory storing state information representing processing to be performed next as claimed in claims 1 and 11 or b) a second (image) processor for executing second (image) processing on (image) data subjected to first (image) processing and a memory for storing state information representing the processing state of the (image) data as claimed in claims 25 and 26, Applicants respectfully request the Examiner withdraws the rejection to claims 1, 11, 25 and 26 under 35 U.S.C. §102(b).

Claims 2-10 and 12-24 depend from claims 1 and 11 and recite additional features. Applicants respectfully submit that claims 2-10 and 12-24 would not have been anticipated by *Kuo et al.* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2-10 and 12-24 under 35 U.S.C. §102(b).

Thus, it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the current set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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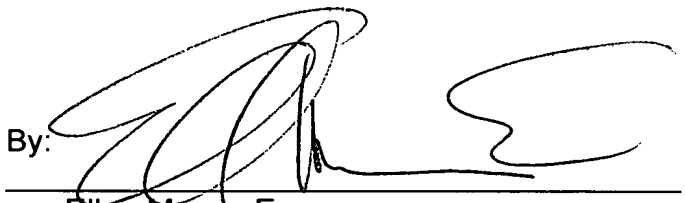
By: 

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